Amendments to the Specification

Please replace paragraph [0020] using paragraph numbers in the application as filed with the following amended paragraph:

[0020] For the computer systems 13 of FIG. 1, source code 8, programmed in a convenient language, represents many application and other programs that collectively constitute a large investment in time and knowledge for owners of native computer systems. The native system 13-1 has available well-perfected compilers/assemblers 9 for forming native executable code 10 [[11]] (legacy code) that efficiently executes application and other programs on the native system 13-1. For the computer systems 13-2, ..., 13-F, however, well-perfected compilers/assemblers may not be available or, even if available, the source code 8 may not always be available. In order to help preserve the investment in the application and other programs of the native computer system, emulators are employed to execute the executable legacy code on one or more of the target computer systems 13-2, ..., 13-F. Typically, the target computer systems 13-2, ..., 13-F are new computer systems that have a different architecture. The objective is to preserve the investment in the application and other programs of the native architecture by enabling them to execute by emulation on the target computer systems.

Please replace paragraph [0022] using paragraph numbers in the application as filed with the following amended paragraph:

[0022] In FIG. 2, further details of the host system 16 of FIG. 1 are shown. The group access unit 11 accesses legacy code (LC) and presents the legacy code in groups (LC_G) to a legacy code translator 21. The legacy code translator 21 stores detailed information about the translation in translation store 24. The legacy code translator 21 also stores the executable blocks of host code in a translated code (TC) cache 23. Legacy features and modes of operation are defined by Program Execution Information 26.

Please replace paragraph [0032] using paragraph numbers in the application as filed with the following amended paragraph:

[0032] In CISC block [[3C-0F]] 3_C-0F, the TM CISC instruction at 0F0 checks a flag in memory, PERFLAG, to determine whether PER is to be enabled. If not, the BNE instruction at 0F4 branches directly to START in CISC block 3_C-10. Otherwise, the SSM instruction at 0F8 sets the PER bit, ENBLPER, in the PSW and the LCTL instruction 0FC sets the store PER bit, STOREPER, in the CR9 control register thereby specifying that all store addresses be matched against the address range indicated in control registers CR10 and CR11.